PATENT ABSTRACTS OF JAPAN

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(21)Application number : 05-135114 (71)Applicant : CANON INC

(22)Date of filing : 14.05.1993 (72)Inventor : HIRAMATSU MAKOTO

(54) INFORMATION REPRODUCING DEVICE

(57)Abstract:

PURPOSE: To reduce a cost by sampling a regenerative signal with a clock signal obtained in a voltage control means and forming a reproducing clock for detecting regenerative data based on the clock signal.

CONSTITUTION: The output of a D/A converter 13 is outputted to a VCO as a signal according to a phase difference between the regenerative signal and the clock signal, similar to the phase comparison signal of a phase comparator in an analog circuit. In the VCO, an oscillation frequency is controlled according to an inputted level difference signal, and a sampling clock for sampling the regenerative signal is outputted. Further, the sampling clock is frequency dimultiplexed to double by a frequency divider 9, and a regenerative clock is generated. The obtained regenerative clock is outputted to a data detection circuit 4, and the regenerative data 5 are detected using the regenerative clock in the data detection circuit 4. In such a case, the regenerative clock is extracted without necessitating the sampling of ten times or above of a data clock, and thus, a cost is reduced.

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CLAIMS

[Claim(s)]

[Claim 1] It is the information regenerative apparatus which digitizes the regenerative signal read from the information record medium, performs signal processing, and detects playback data. The edge detection means for detecting that the digital data which sampled said regenerative signal and was obtained is within the limits of predetermined to slice level, and detecting the edge to the slice level of a regenerative signal, The level difference detection means for detecting the digital data in the location of the edge detected with this edge detection means, and the difference of said slice level, While sampling said regenerative signal with the clock signal which was equipped

with the armature-voltage control oscillation means by which the oscillation frequency of a clock signal is controlled according to the level difference detected with this level difference detection means, and was acquired with this armature-voltage control oscillation means The information regenerative apparatus characterized by creating the clock for playback for detecting said playback data based on said clock signal.

[Claim 2] Said clock for playback is the information regenerative apparatus of claim 1 which carries out dividing of said clock signal, or is characterized by remaining as it is and creating a clock signal as a clock for playback.

[Claim 3] The frequency of the clock signal created as said object for a sampling is the information regenerative apparatus of claim 1 characterized by being 2 double less or equal of the data clock which playback data have.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the information regenerative apparatus which reproduces the information recorded on the information record medium.

[0002]

[Description of the Prior Art] Conventionally, when reproducing information in an information record regenerative apparatus, analogically, waveform equalization of the regenerative signal read from the record medium is carried out, and it is made binary after that. And a playback clock is extracted applying PLL after binary-izing, and playback data are detected using the obtained playback clock. The block diagram in which drawing 6 showed an example of such a data regenerative apparatus, and drawing 7 are the signal waveform diagrams having shown the signal of each part of drawing 6 . Hereafter, the conventional data regenerative apparatus is explained based

on drawing 6 and drawing 7 . 101 in drawing is the regenerative signal read from information record media, such as an optical disk, and after waveform equalization is carried out as mentioned above in a waveform equalization circuit 102, it is made binary with slice level predetermined in the binary-ized circuit 103. If drawing 7 (a) shows the regenerative signal read from the record medium and makes this binary with predetermined slice level after waveform equalization, a binary-ized signal as shown in drawing 7 (b) will be generated.

[0003] A binary-ized signal is inputted into the PLL circuit 108, and the playback clock 109 as shown in drawing 7 (c) is extracted by comparing a binary-ized signal with a phase here. Moreover, in the data detector 104, the playback data 105 are generated by detecting a binary-ized signal with a playback clock. In addition, before a regenerative signal is inputted, a playback clock is controlled by the control signal sent from the main control circuit which does not illustrate the PLL circuit 108 to lock in a reference clock. Drawing 8 is the block diagram having shown the concrete configuration of the PLL circuit 108, and 110 is a change-over switch controlled by the control signal 107. When the mode of operation in the condition, i.e., equipment, that the regenerative signal 101 is not inputted is not a playback mode, it is that connect with the b side with the control signal 107, and a change-over switch 110 inputs a reference clock 106 into the phase comparator 111 of the PLL circuit 108, and the playback clock 109 is locked by the reference clock 106. And if a mode of operation turns into a playback mode, a change-over switch 110 will be connected to the a side by the control signal 107, and a binary-ized signal will be inputted into a phase comparator 111.

[0004] In a phase comparator 111, the playback clock 109 of drawing 7 (c) is compared with the phase of a binary-ized signal, and the phase-comparison signal which shows the phase contrast of two signals as shown in drawing 7 (d) is generated. The acquired phase-comparison signal is outputted to the charge pump circuit 112, and is changed into the signal of the electrical-potential-difference value which is proportional to phase contrast as shown in drawing 7 (e). The output signal of the charge pump circuit 112 is further outputted to VCO (Voltage Controll Oscilater) 113, and the playback clock 109

is extracted by changing a frequency in proportion to the electrical potential difference of a charge pump output here. In this way, in the PLL circuit 108, the playback clock 109 is generated and playback data are generated using the playback clock 109 as mentioned above in the data detector 104.

[0005]

[Problem(s) to be Solved by the Invention] In the conventional information record regenerative apparatus, when it is exchanged in an information record medium or an informational transfer rate is changed, in order that the grace and frequency characteristics of a regenerative signal may change, the property of a waveform equalization circuit must also be changed. However, in the above-mentioned conventional data regenerative apparatus, in order to carry out waveform equalization of the regenerative signal in analog, circuitry was complicated to change the property of waveform equalization and there was a problem of causing the cost rise of equipment in it. Then, by the extract approach of a playback clock like before, although how to carry out A/D conversion of the regenerative signal, and to detect playback data and a playback clock by digital signal processing as solution of this problem could be considered, when it was going to compare a phase in digital one, since the sampling clock of 10 times or more of a data clock was required, the high-speed A/D converter was needed and there was a problem of causing a cost rise on the contrary.

[0006] This invention was made in order to cancel such a trouble, it enables it to extract a playback clock, without requiring a high-speed A/D converter, and aims at offering the information regenerative apparatus into which the waveform-equalization property of a regenerative signal was simply changed by this by digital signal processing.

[0007]

[Means for Solving the Problem] The purpose of this invention is an information regenerative apparatus which digitizes the regenerative signal read from the information record medium, performs signal processing, and detects playback data. The edge detection means for detecting that the digital data which sampled said regenerative signal and was obtained is within the limits of predetermined to slice level, and detecting the edge to the slice level

of a regenerative signal, The level difference detection means for detecting the digital data in the location of the edge detected with this edge detection means, and the difference of said slice level, While sampling said regenerative signal with the clock signal which was equipped with the armature-voltage control oscillation means by which the oscillation frequency of a clock signal is controlled according to the level difference detected with this level difference detection means, and was acquired with this armature-voltage control oscillation means It is attained by the information regenerative apparatus characterized by creating the clock for playback for detecting said playback data based on said clock signal.

[0008]

[Example] Hereafter, the example of this invention is explained to a detail with reference to a drawing. Drawing 1 is the block diagram having shown one example of the information regenerative apparatus of this invention. In drawing 1 , 2 is an A/D converter for sampling the regenerative signal 1 read from the information record medium by the predetermined sample takeoff point, and changing into a digital signal. A regenerative signal 1 is a signal optically reproduced from information record media, such as an optical disk which is not illustrated, and is changed into a digital data signal train from an analog signal based on the reference voltage directed from CPU11 with A/D converter 2. The waveform equalization circuit where 3 consisted of digital filters, and 4 are the data detectors for comparing the slice level given from the data and CPU11 of a waveform equalization circuit 3, and detecting the playback data 5. CPU11 controls the whole equipment, as mentioned above, slice level is outputted to reference voltage at A/D converter 2, and is outputted to a waveform equalization circuit 3 in a filter coefficient and the data detector 4, and an AGC (Auto Gain Controll) property, a waveform-equalization property, and a data detection property are controlled by this, respectively. A PLL circuit for 8 to extract a sampling clock and 9 are the counting-down circuits for carrying out dividing of the sampling clock of the PLL circuit 8, and generating the playback clock 10. A reference clock 6 and the control signal 7 are sent to the PLL circuit 8 from the main control circuit which is not illustrated.

[0009] Drawing 2 is the block diagram having shown the concrete configuration of the PLL circuit 8. While 12 is a level detector which has a phase-comparison function and detecting the edge to the slice level of the data of the sampled regenerative signal in drawing 2 , the phase contrast over the sampling clock of a regenerative signal is detected. A D/A converter for 13 to change the output of the level detector 12 into an analog signal and 16 are change-over switches controlled by the control signal 7. Moreover, as for a phase comparator and 15, 14 is [a charge pump circuit and 17] VCO (voltage controlled oscillator), and each of these is the same as what was shown in drawing 8 .

[0010] Next, actuation of the above-mentioned example is explained based on the timing diagram of drawing 3 . First, when the mode of operation in the condition, i.e., equipment, that the regenerative signal is not inputted is not a playback mode, a change-over switch 16 is connected to the b side by the control signal 7. Therefore, a reference clock 6 is inputted into a phase comparator 14 at this time, and a playback clock is locked by the reference clock 6 as usual. On the other hand, if the mode of operation of equipment turns into a playback mode, a change-over switch 16 will be switched to the a side by the control signal 7. By this, as shown in drawing 3 (a), the regenerative signal by which waveform equalization was carried out in the waveform equalization circuit 3 is sampled by the sample takeoff point shown by the black dot, and it is incorporated as a digital data train in the level detector 12. A regenerative signal is sampled by the sampling clock of drawing 3 (b).

[0011] It is [as opposed to / as the level detector 12 shows to drawing 3 (a) / the slice level of a regenerative signal] electrical-potential-difference range V1 -V2 predetermined. When it is decided and a regenerative signal is in this electrical-potential-difference range, the edge to the slice level of a regenerative signal is detected. Moreover, in the level detector 12, in the detected edge location, the difference of regenerative-signal data and slice level is detected, and as the acquired signal shows drawing 3 (c), it is outputted to D/A converter 13 as a level difference detecting signal. In D/A converter 13, the output of the level detector 12 is changed into an analog

signal, and as shown in drawing 3 (d), it is outputted to VCO17 through a change-over switch 16 as an analog signal according to a level difference.

[0012] In this case, it is ******(ed) whether the phase of the edge to the slice level of a regenerative signal being a rising edge, and being a falling edge, i.e., a regenerative signal, is progressing to a sampling clock and whether it is from the sampling clock before and behind the output signal of the level difference detector 12 of drawing 3 (c) behind, and the output of D/A converter 13 is reversed according to that result. That is, the output of D/A converter 13 is outputted to VCO17 as a signal according to the phase contrast of a regenerative signal and a clock signal like the phase-comparison signal of the phase comparator of an analog circuit. An oscillation frequency is controlled by VCO17 according to the inputted level difference signal, and it is outputted as a sampling clock for sampling a regenerative signal. Moreover, it doubles dividing of this sampling clock with a counting-down circuit 9, and a playback clock is generated as shown in drawing 3 (e). The obtained playback clock is outputted to the data detector 4, and the playback data 5 are detected in the data detector 4 using a playback clock.

[0013] When the digital data of the sampled regenerative signal is in predetermined electrical-potential-difference within the limits beforehand decided to slice level in this example, while detecting the edge to the slice level of a regenerative signal By having detected the level difference of digital data and slice level in this edge location, having controlled the frequency of VCO according to this level difference, and having controlled the frequency of a sampling clock The phase contrast of a sampling clock is compared for a regenerative signal in digital one, and the PLL function by digital signal processing completely equivalent to the PLL circuit of an analog circuit can be given. Therefore, without requiring the sampling clock of 10 times or more of a data clock, when signal processing of information playback is digitized, a playback clock can be extracted and information playback can be digitized without a high-speed A/D converter. When a waveform equalization circuit is constituted from a digital circuit and it changes a waveform-equalization property especially according to exchange of an information record medium, modification of an informational transfer rate, etc., since the high-speed A/D

converter is unnecessary as mentioned above, digitization becomes possible, without becoming cost quantity. Moreover, when changing the property of a waveform equalization circuit by this digitization, compared with an analog circuit, circuitry can be simplified sharply. Furthermore, in this example, data can be sampled with a clock signal twice [only] the frequency of a data clock.

[0014] Drawing 4 is the block diagram having shown other examples of the information regenerative apparatus of this invention. In drawing 4 , the same part as the example of drawing 1 is made to attach the same sign and to omit explanation. In addition, in this example, NRZI conversion shall be adopted as a record sign. In NRZI conversion, since "1" of record data supports the location of an edge, the location of the edge to the slice level of a regenerative signal is detected by the level detector 12 like the example of drawing 1 and drawing 2 also here that what is necessary is just to detect the location therefore. However, since a sampling clock and the playback clock from data will be in agreement in this example, the frequency of a sampling clock can be further made low.

[0015] Drawing 5 (a) is the regenerative signal of a waveform equalization circuit 3, drawing 5 (b) is a sampling clock, and a regenerative signal is sampled with a sampling clock and incorporated as digital data in the level detector 12 of the PLL circuit 8. Electrical-potential-difference range V1 -V2 the regenerative signal was beforehand decided to be like [in the level detector 12] the example of drawing 1 When it is in between, the edge to the slice level of a regenerative signal is detected. Moreover, in the level detector 12, the level difference of the level and slice level of the regenerative signal in the edge location is detected, and as shown in drawing 5 (c), it is outputted to D/A converter 13 as a level difference detecting signal. In D/A converter 13, as shown in drawing 5 (d), a level difference detecting signal is changed into an analog signal, and like the example of drawing 1 , the output of D/A converter 13 is reversed according to progress of a phase and delay to the extent that it receives the sampling clock of a regenerative signal. The frequency of a clock signal is controlled by VCO17 according to the output of D/A converter 13, and it is outputted as a sampling clock for sampling a regenerative signal. In addition, since the sampling clock and the playback

clock are in agreement here, it is not necessary to carry out dividing and the sampling clock of VCO17 is outputted to the data detector 4 as a playback clock as it is. Thus, also in this example, it becomes possible to apply PLL by digital signal processing completely like the example of drawing 1 , and a playback clock can be extracted, without requiring a high-speed D/A converter.

[0016]

[Effect of the Invention] As explained above, this invention becomes possible [comparing the phase of a regenerative signal and a sampling clock in digital one, and giving the function of a PLL circuit], and a playback clock can be extracted, without requiring the clock of 10 times or more of a data clock like before by this. Therefore, when signal processing of information playback is digitized, it is effective in a waveform-equalization property being changeable, without being an easy configuration compared with an analog circuit, and becoming cost quantity, when a high-speed A/D converter is not required and a waveform equalization circuit is constituted from a digital circuit.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram having shown one example of the information regenerative apparatus of this invention.

[Drawing 2] It is the block diagram having shown the concrete configuration of the PLL circuit of drawing 1 .

[Drawing 3] It is the timing diagram which showed actuation of the example of drawing 1 .

[Drawing 4] It is the block diagram having shown other examples of this invention.

[Drawing 5] It is the timing diagram which showed actuation of the example of drawing 4 .

[Drawing 6] It is the block diagram having shown the information regenerative

apparatus of the conventional example.

[Drawing 7] It is the timing diagram which showed actuation of the equipment of drawing 6 .

[Drawing 8] It is the block diagram having shown the PLL circuit of drawing 6 in the detail.

[Description of Notations]

2 A/D Converter

3 Waveform Equalization Circuit

4 Data Detector

8 PLL Circuit

9 Counting-down Circuit

11 CPU

12 Level Detector

13 D/A Converter

14 Phase Comparator

15 Charge Pump Circuit

16 Change-over Switch

17 VCO (Voltage Controlled Oscillator)